



Radxa X4

schematic

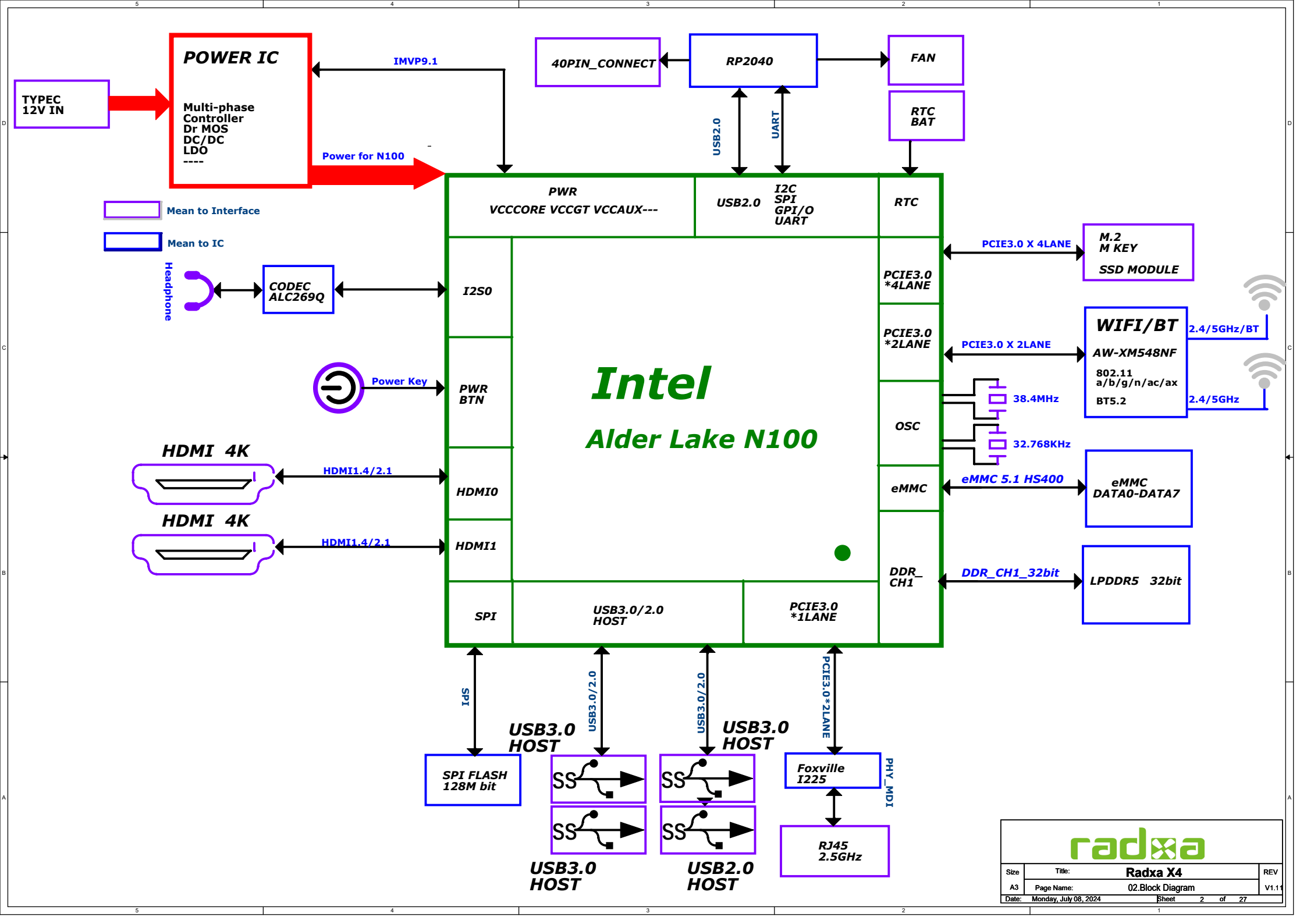
V1.11

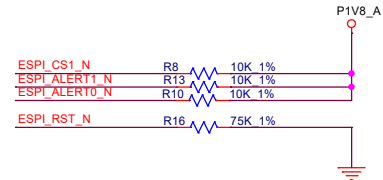
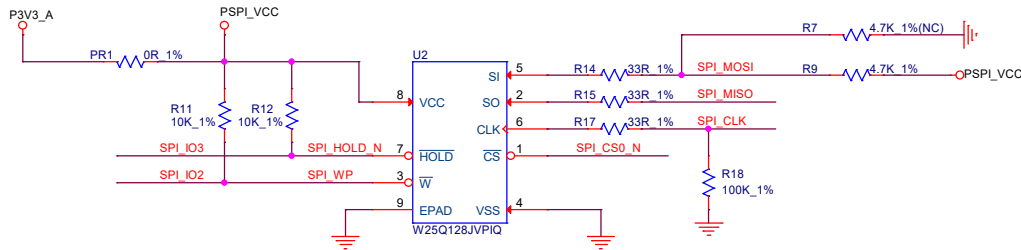
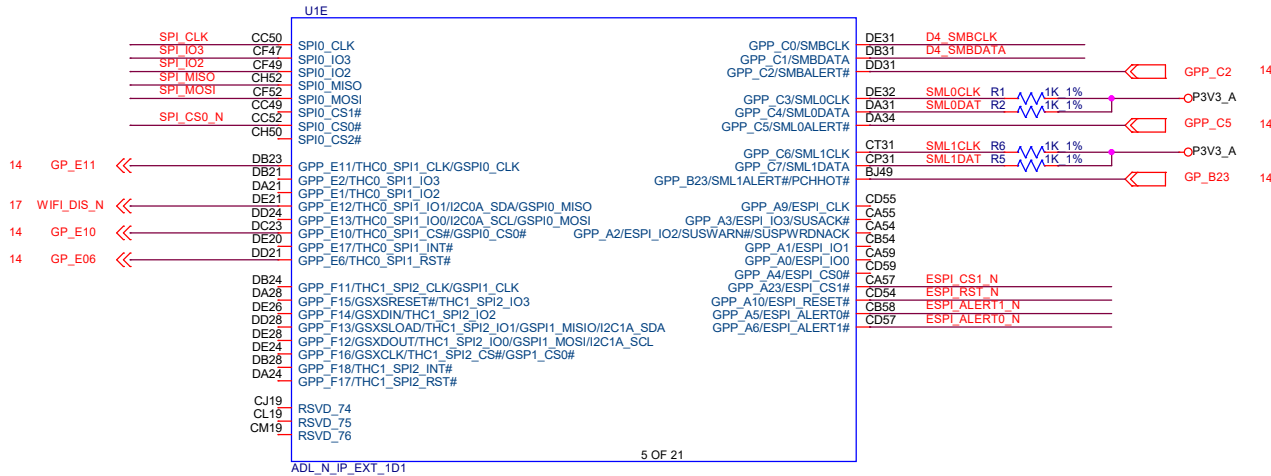


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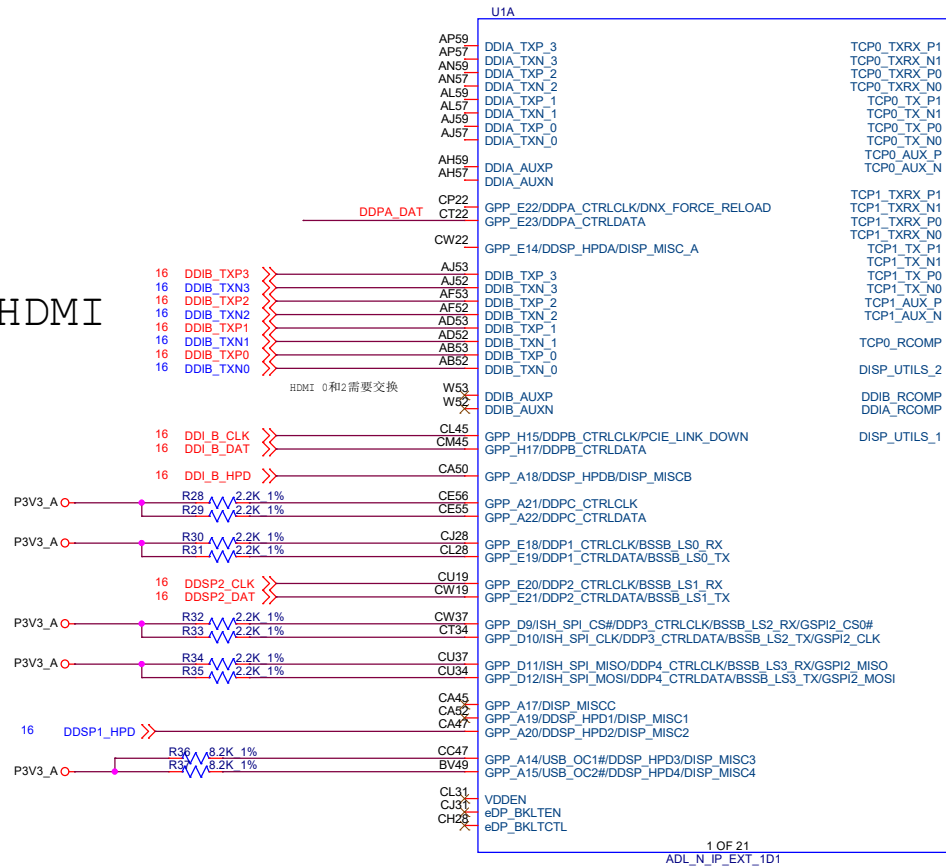
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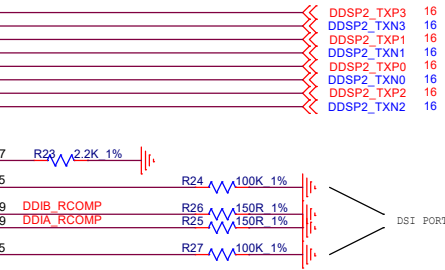




HDMI



DP++

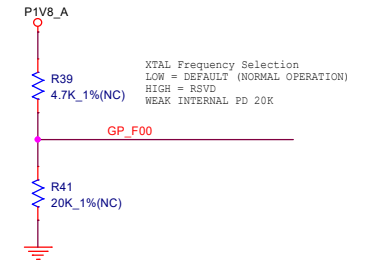


TCP Port Signal Mapping for HDMI / DP

TCP	HDMI	DP
TX0	DATA2	LANE0
TX1	DATA0	LANE2
TXRX0	DATA1	LANE1
TXRX1	CLK	LANE3

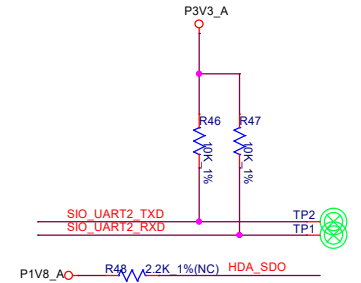
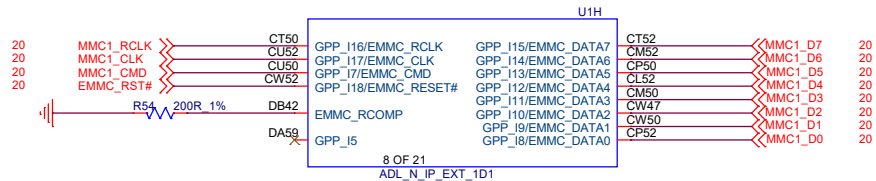
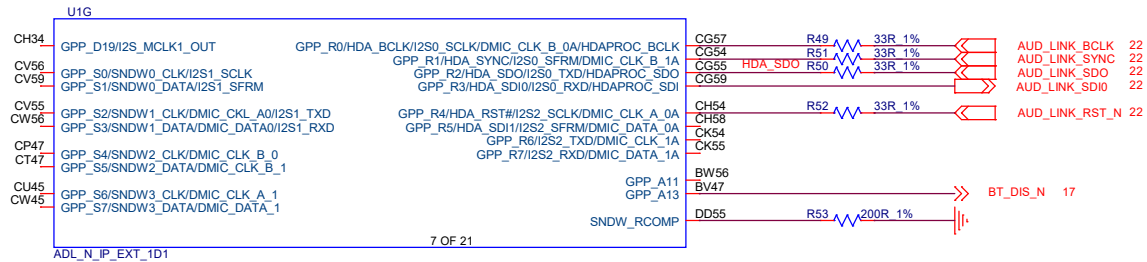
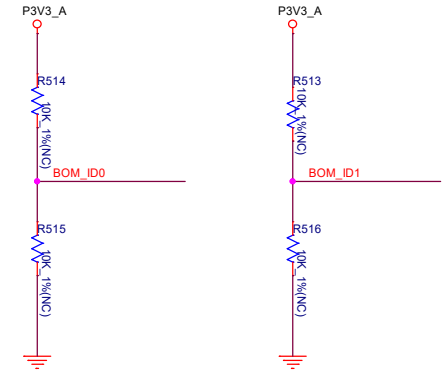
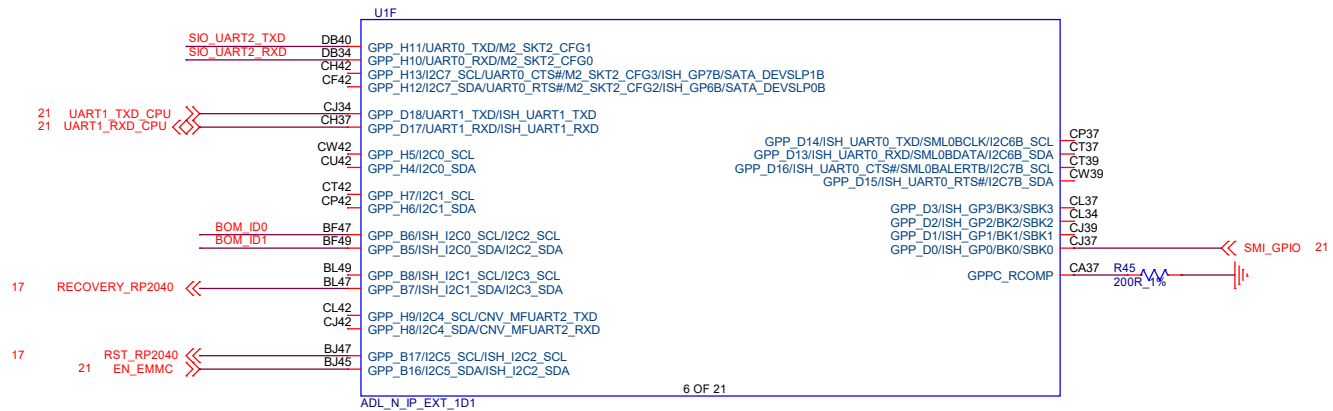
DDI Port Signal Mapping for HDMI / DP

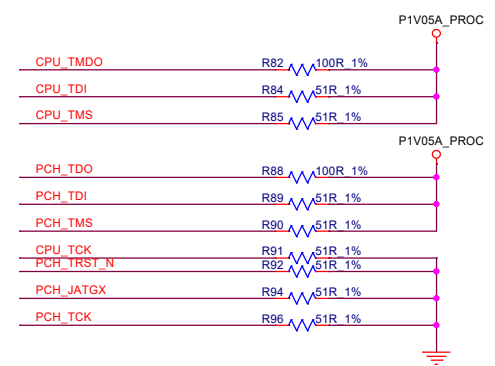
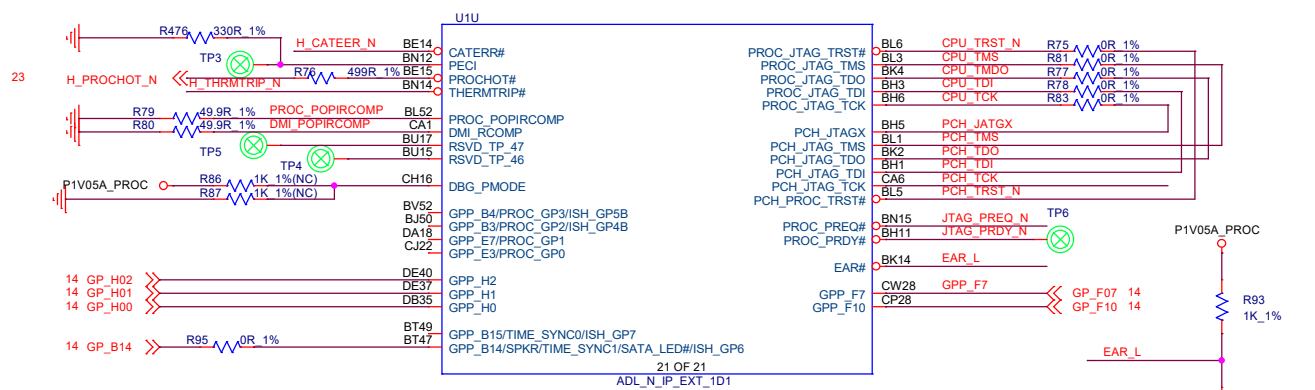
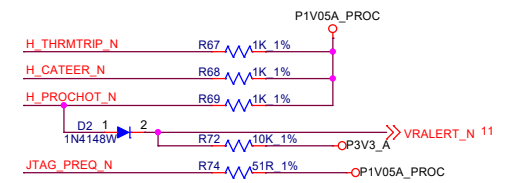
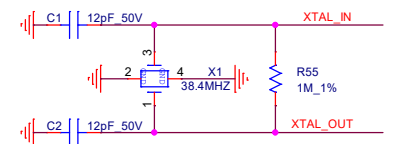
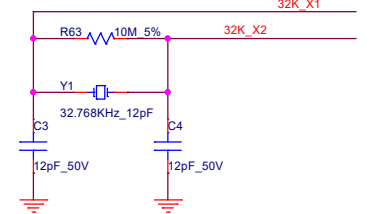
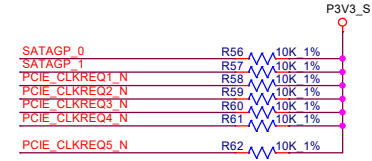
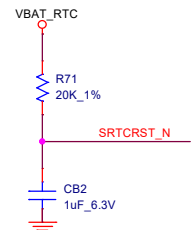
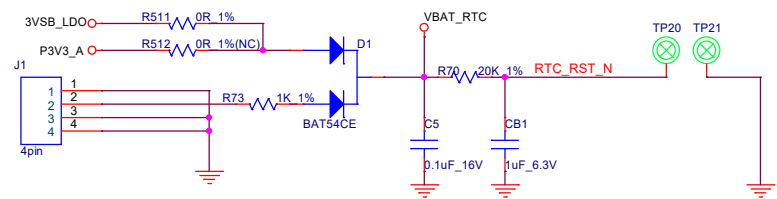
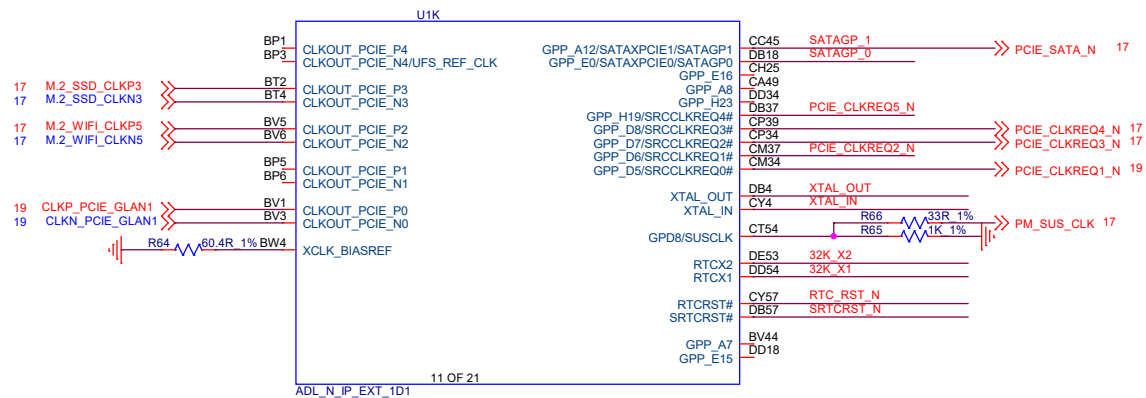
DDI	HDMI
TX0	DATA2
TX1	DATA1
TX2	DATA0
TX3	CLK



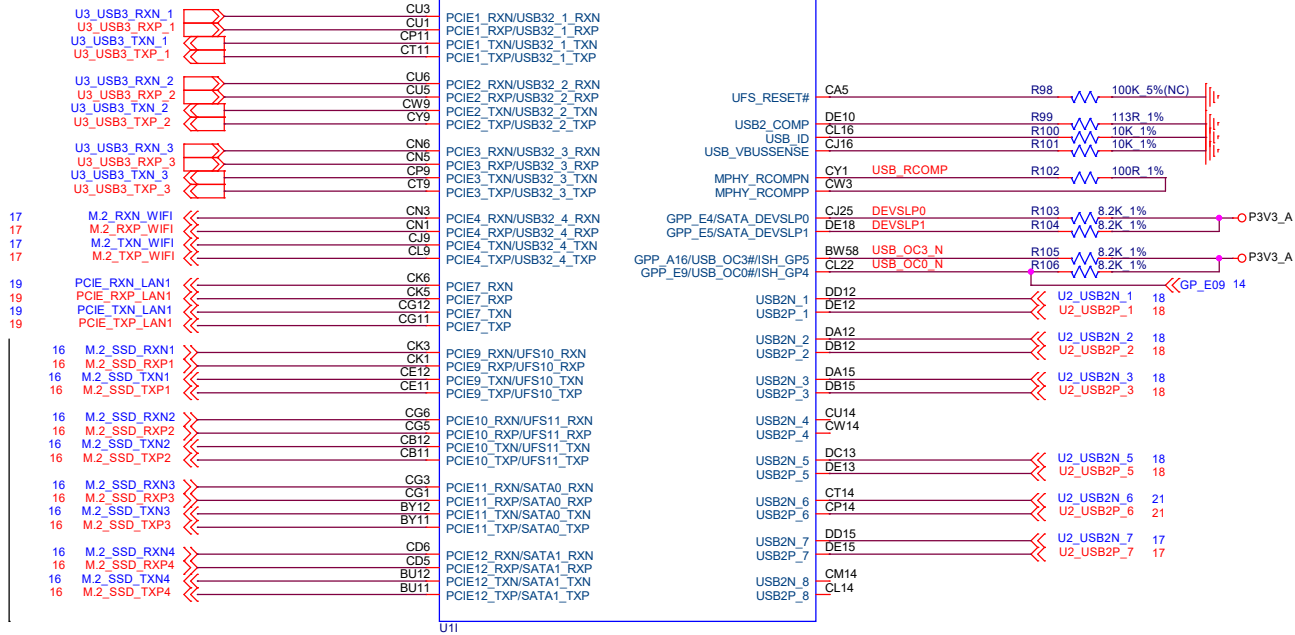
M.2 CNVI MODES
LOW-> INTEGRATED CNVI ENABLE
HIGH-> INTEGRATED CNVI DISABLE
NO INTERNAL PU/PD
SAMPLING - RSMRSTB

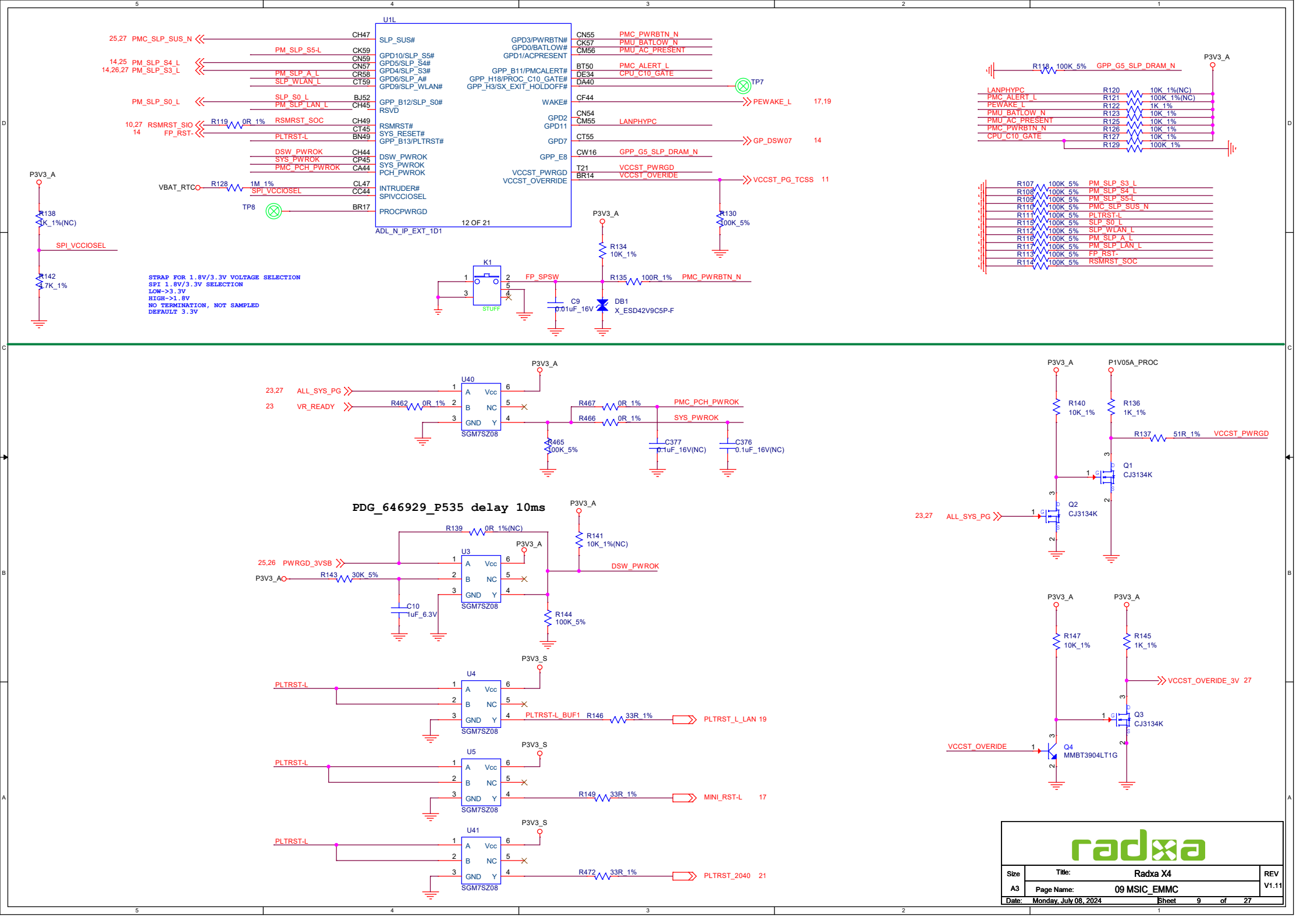


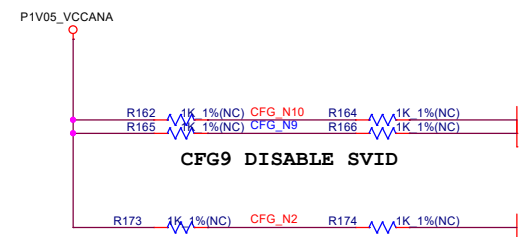




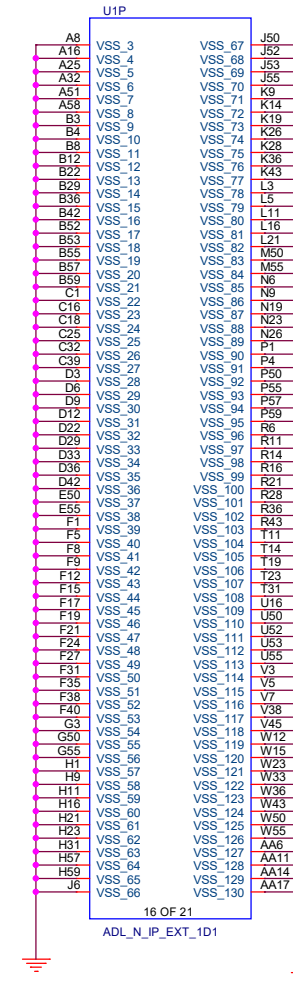
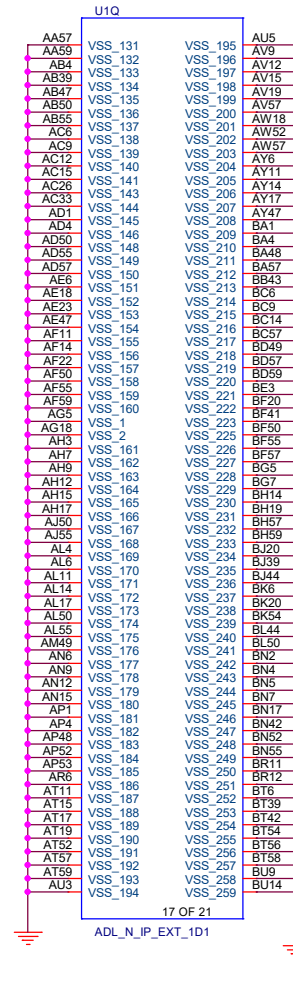
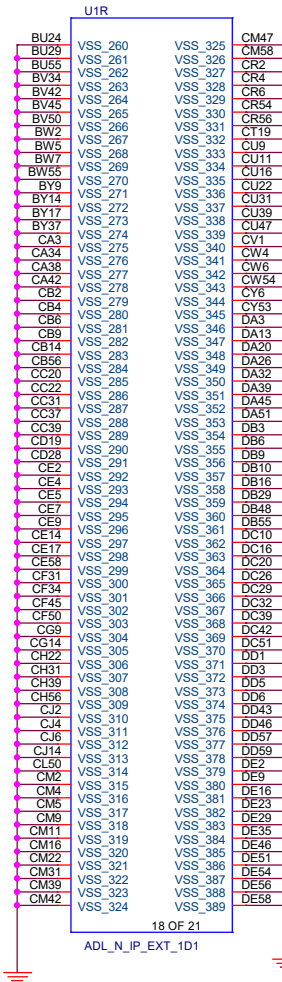
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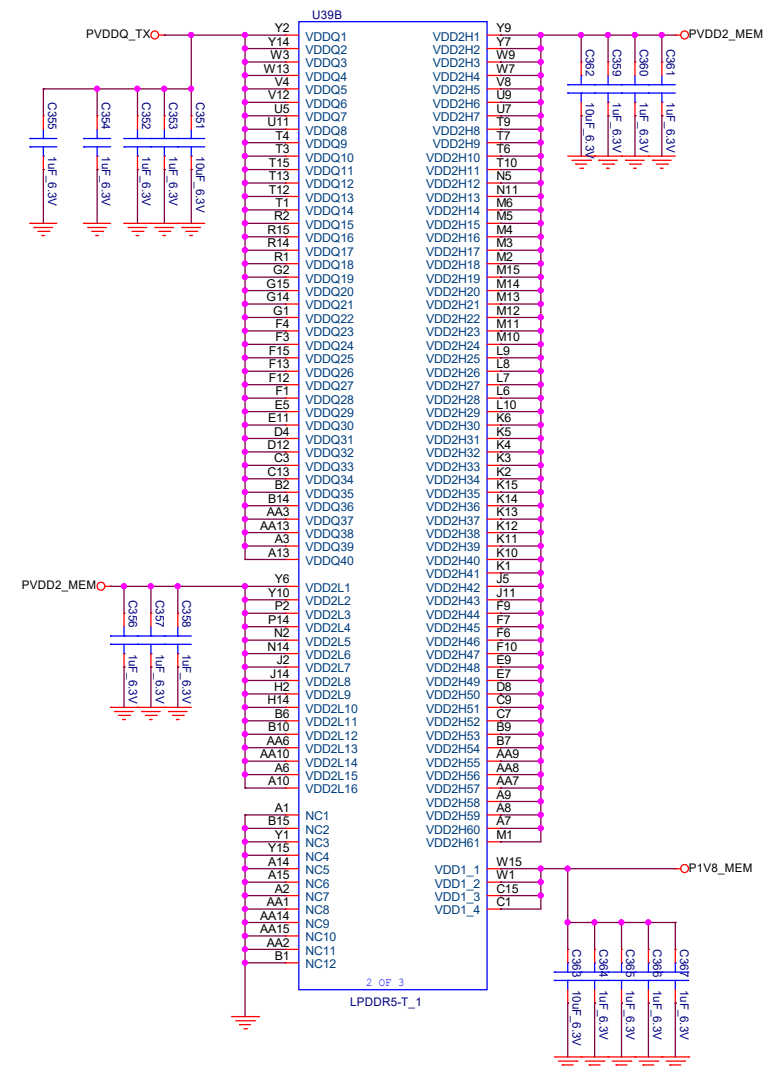
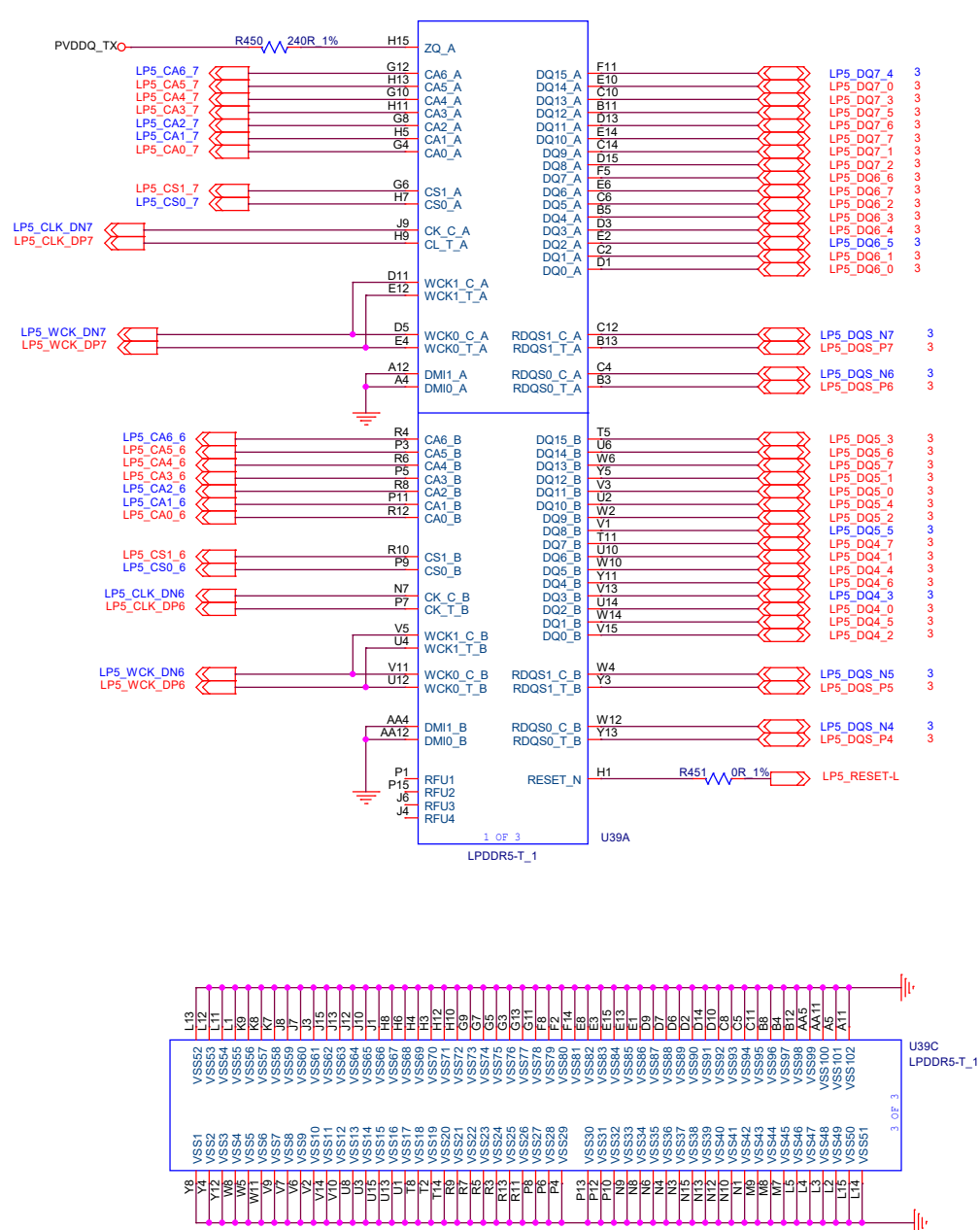


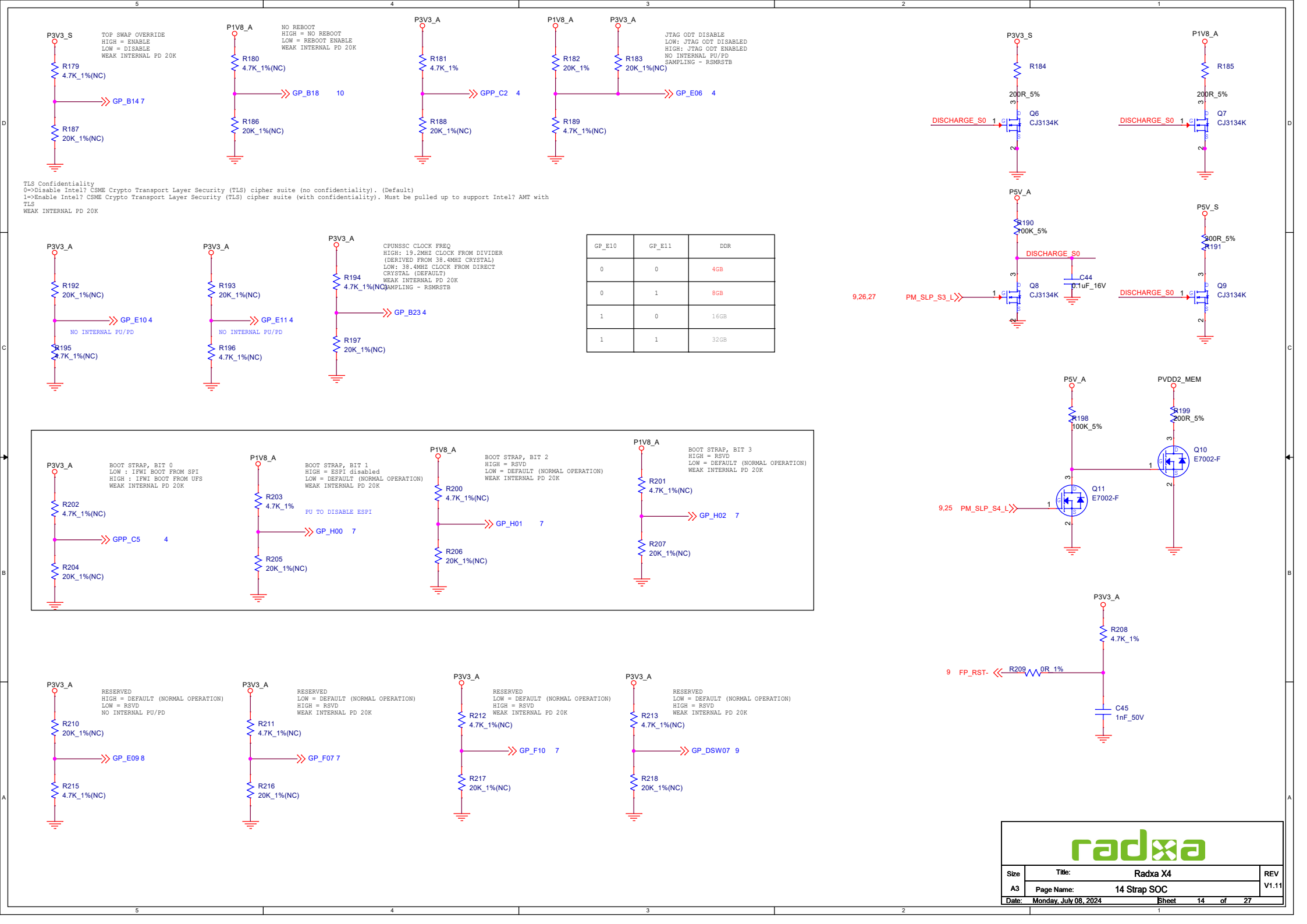


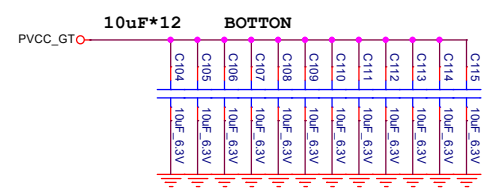
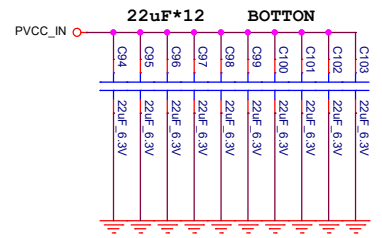
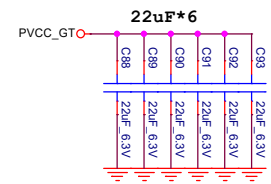
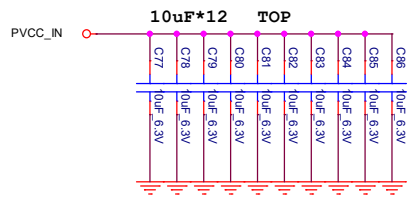
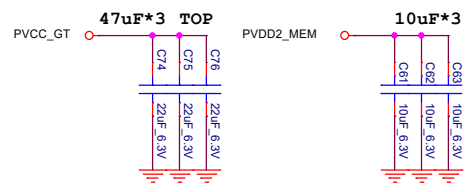
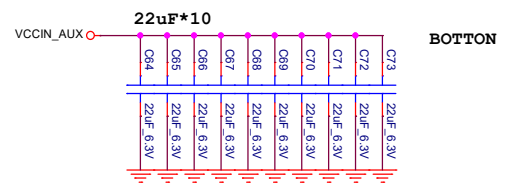
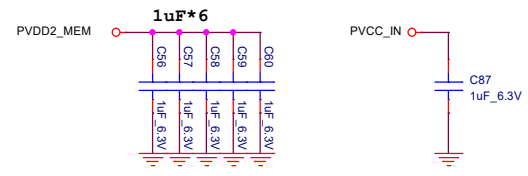
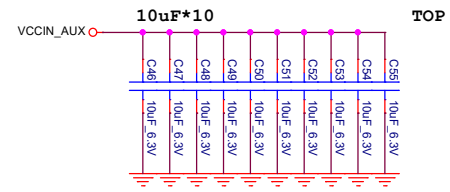


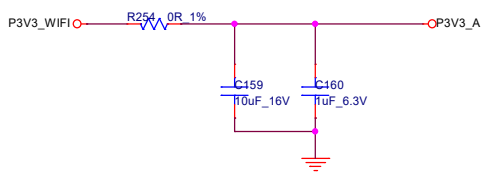
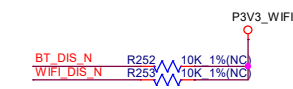
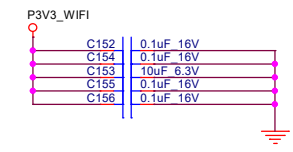
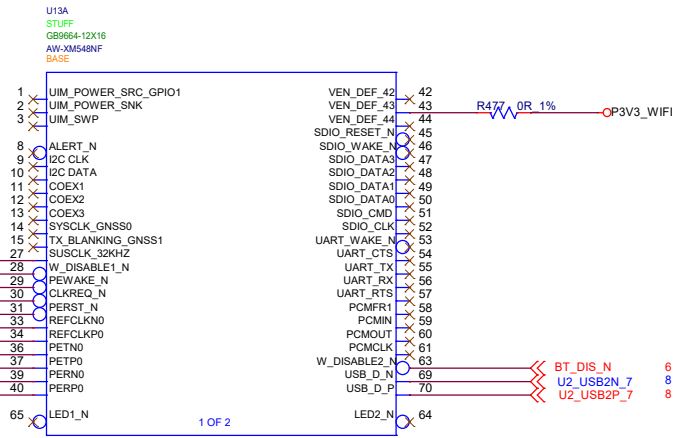
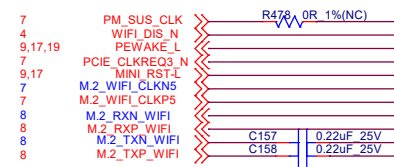
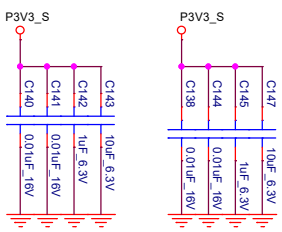
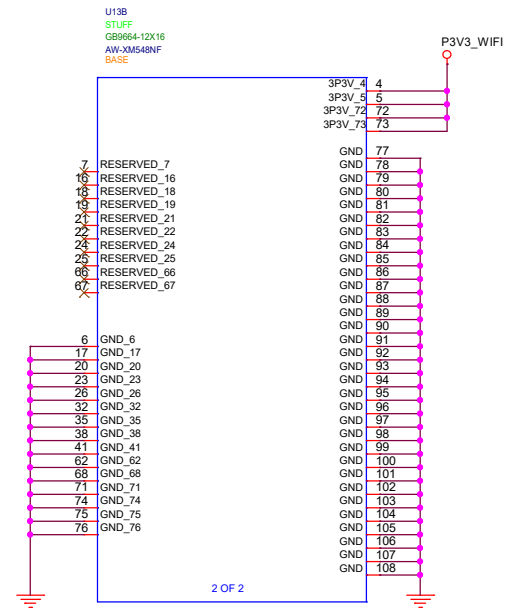
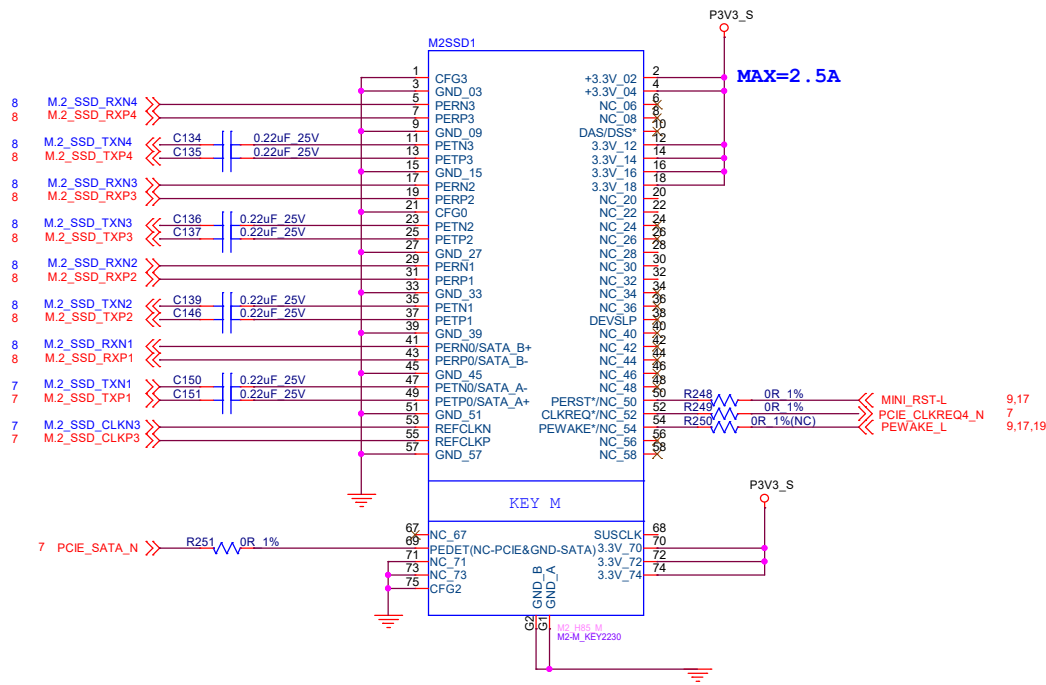
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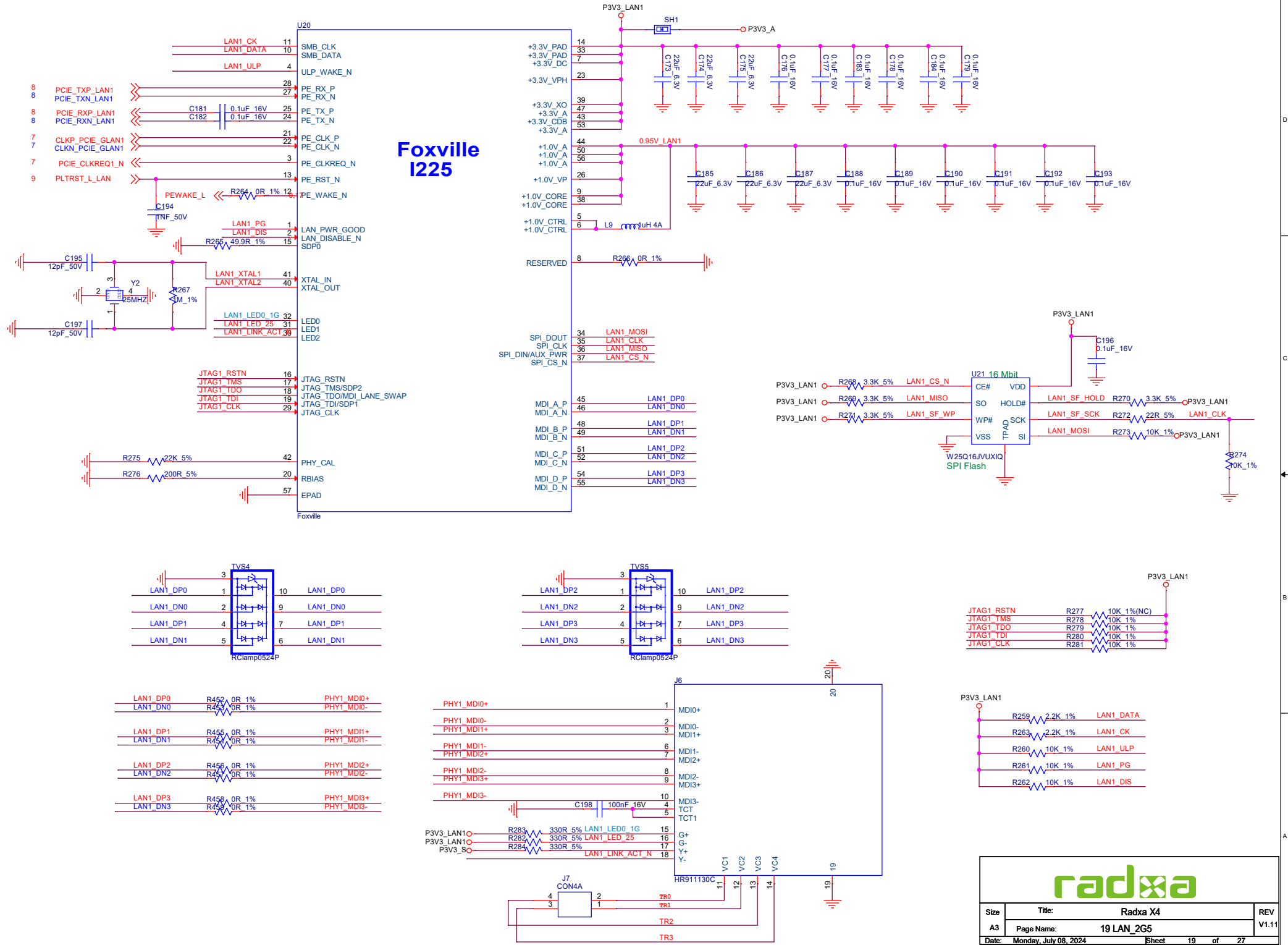






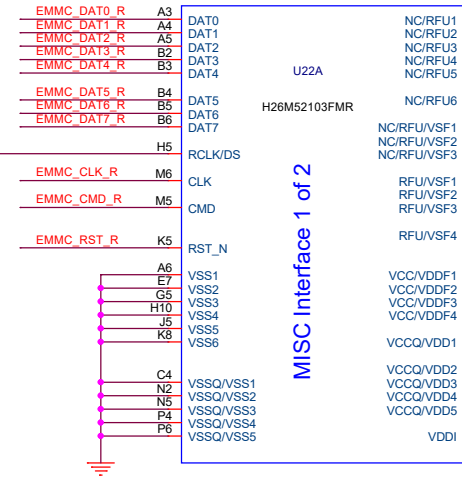
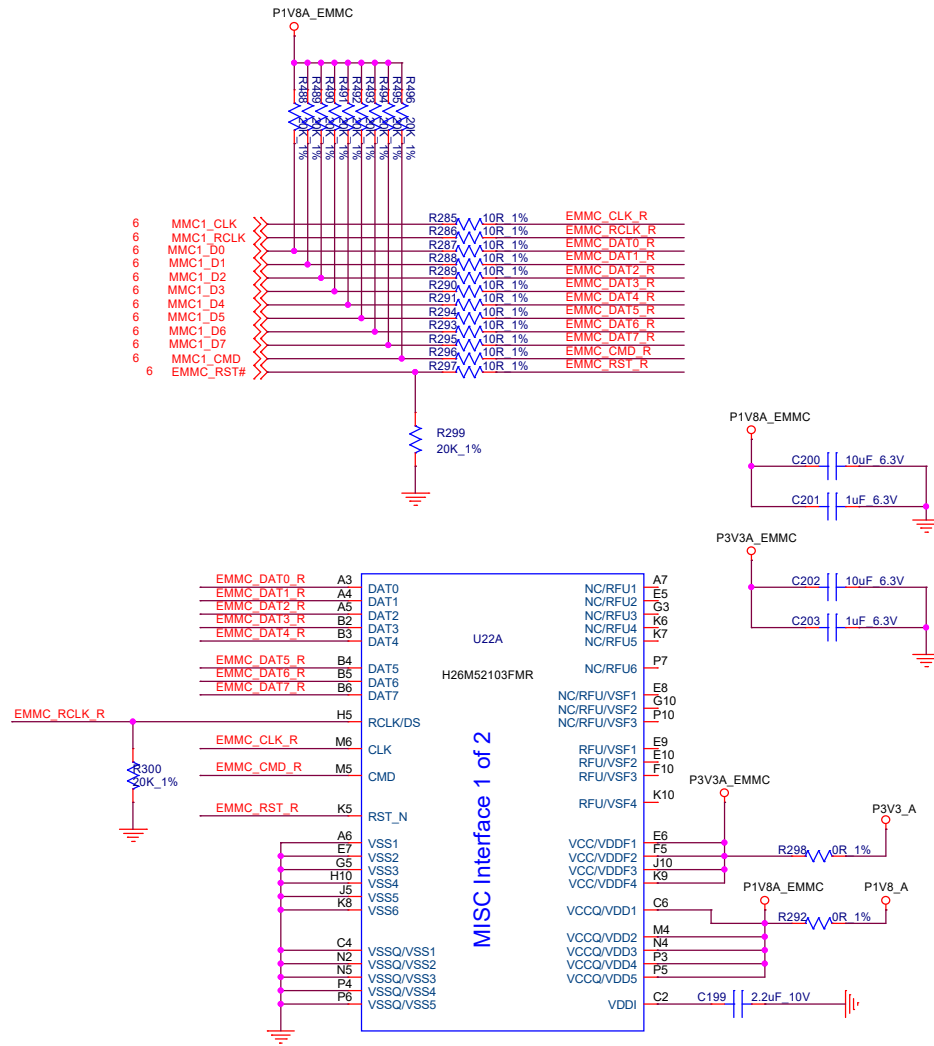




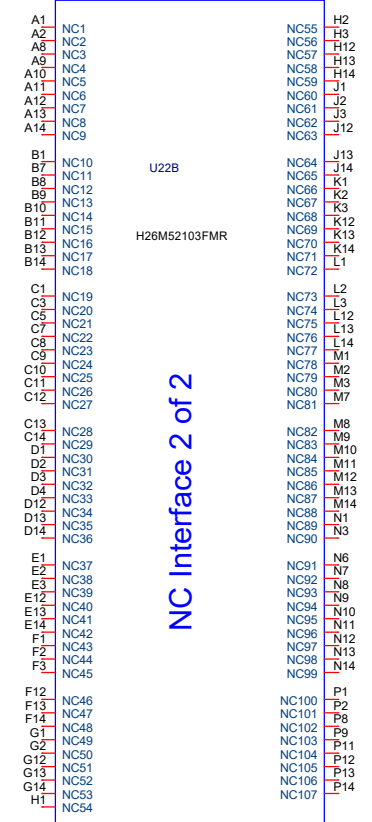


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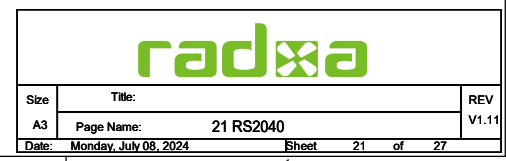
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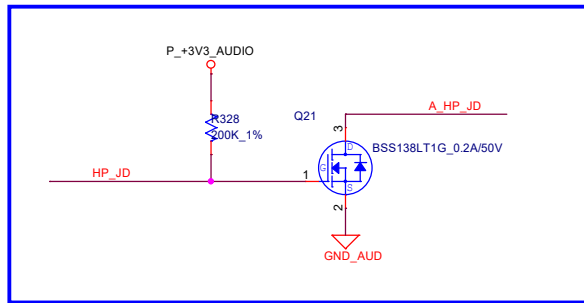


MISC Interface 1 of 2

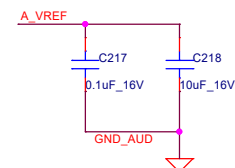
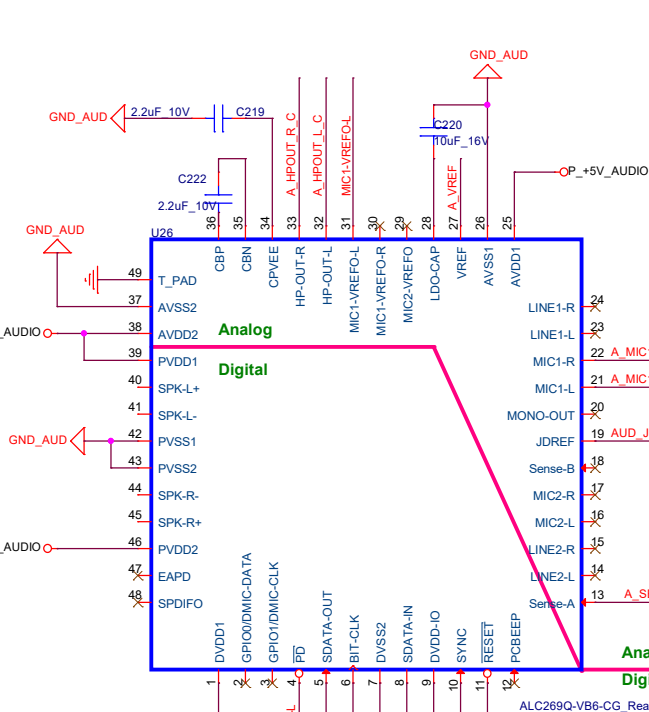
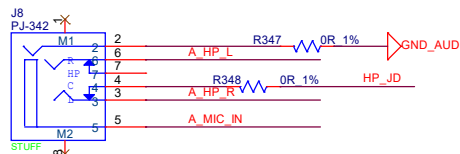
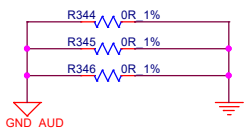
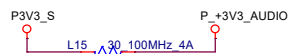
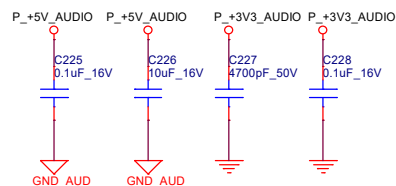
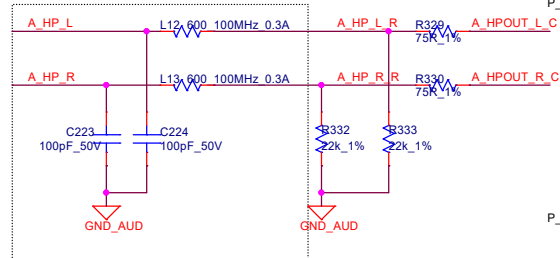


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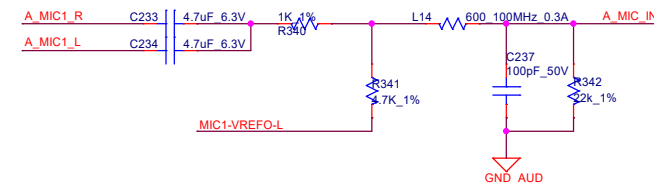
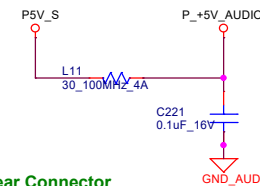




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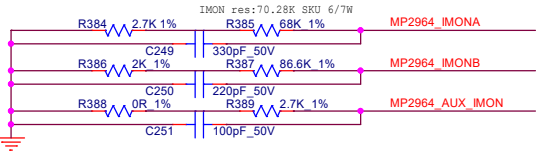
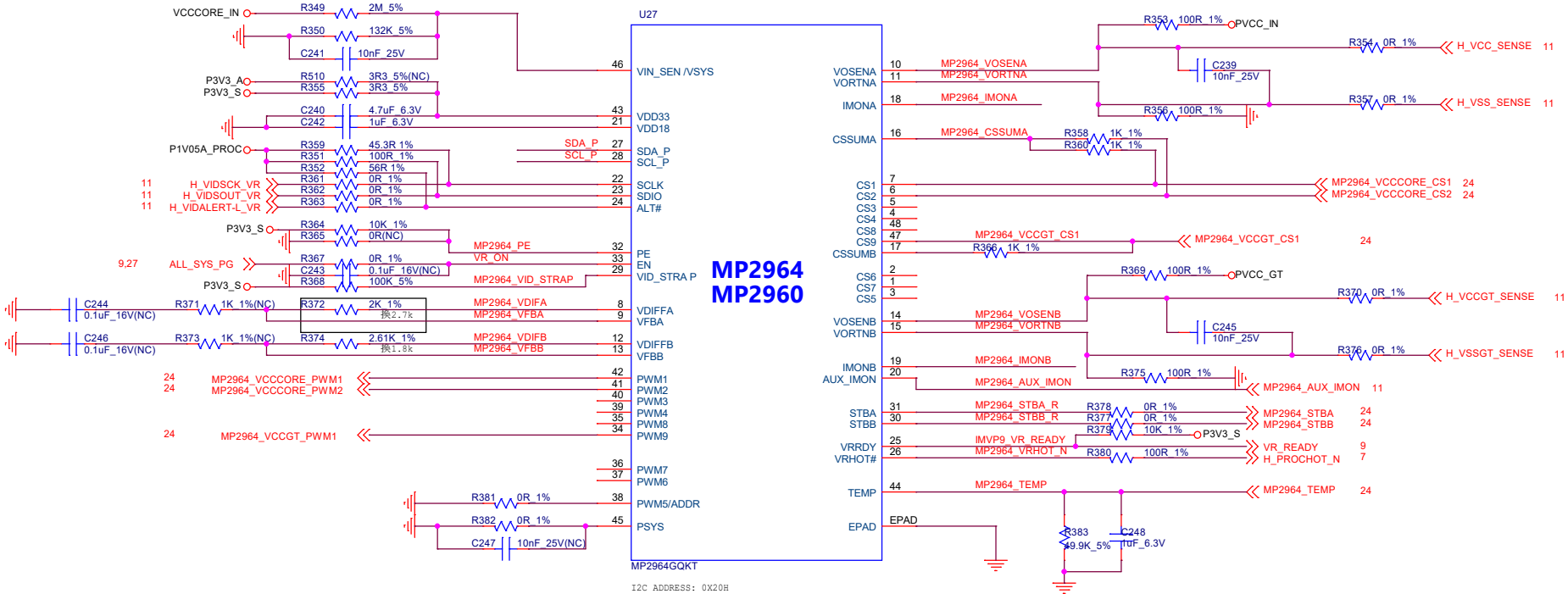
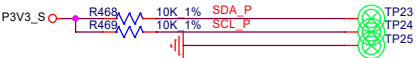
Near Connector



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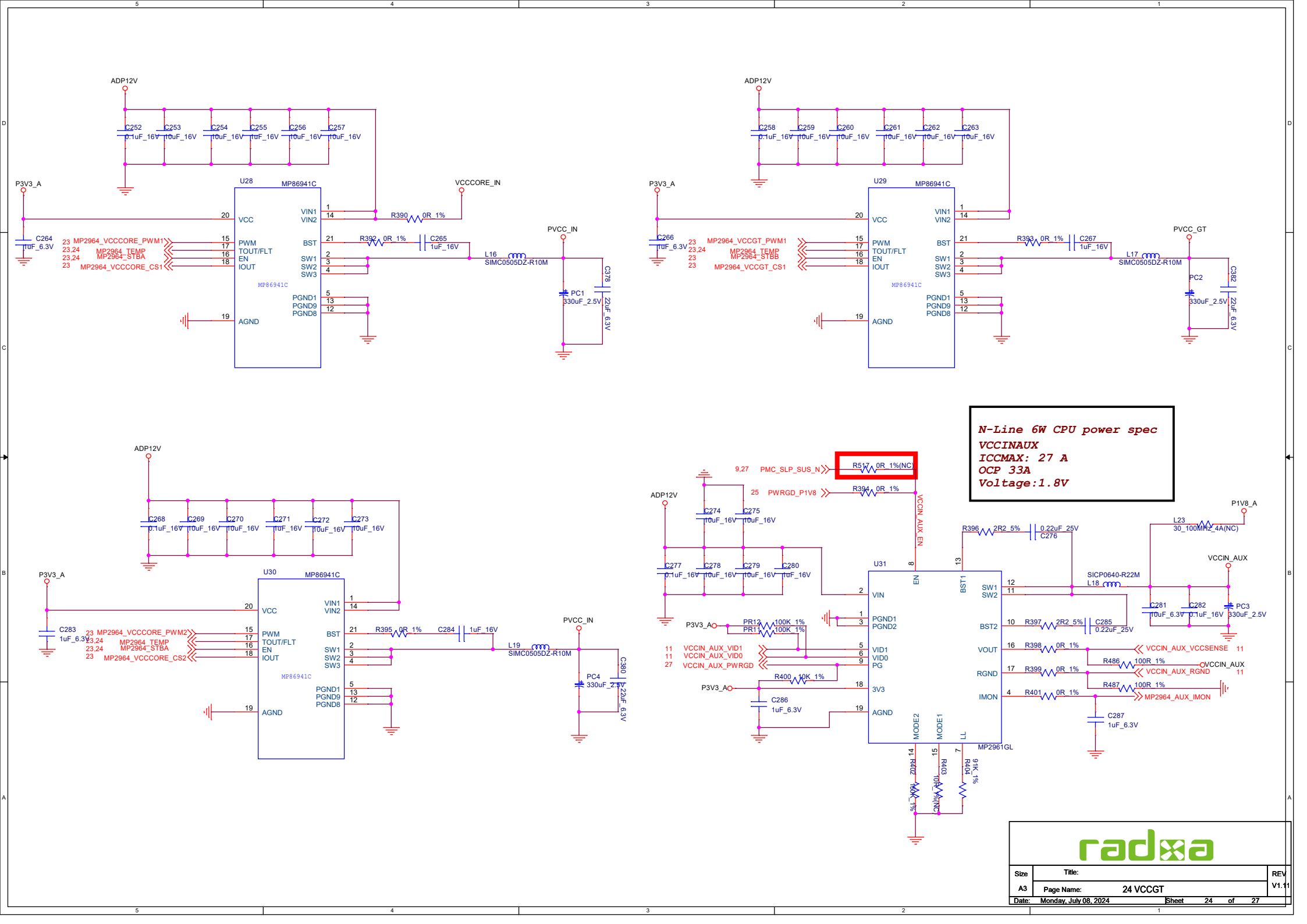
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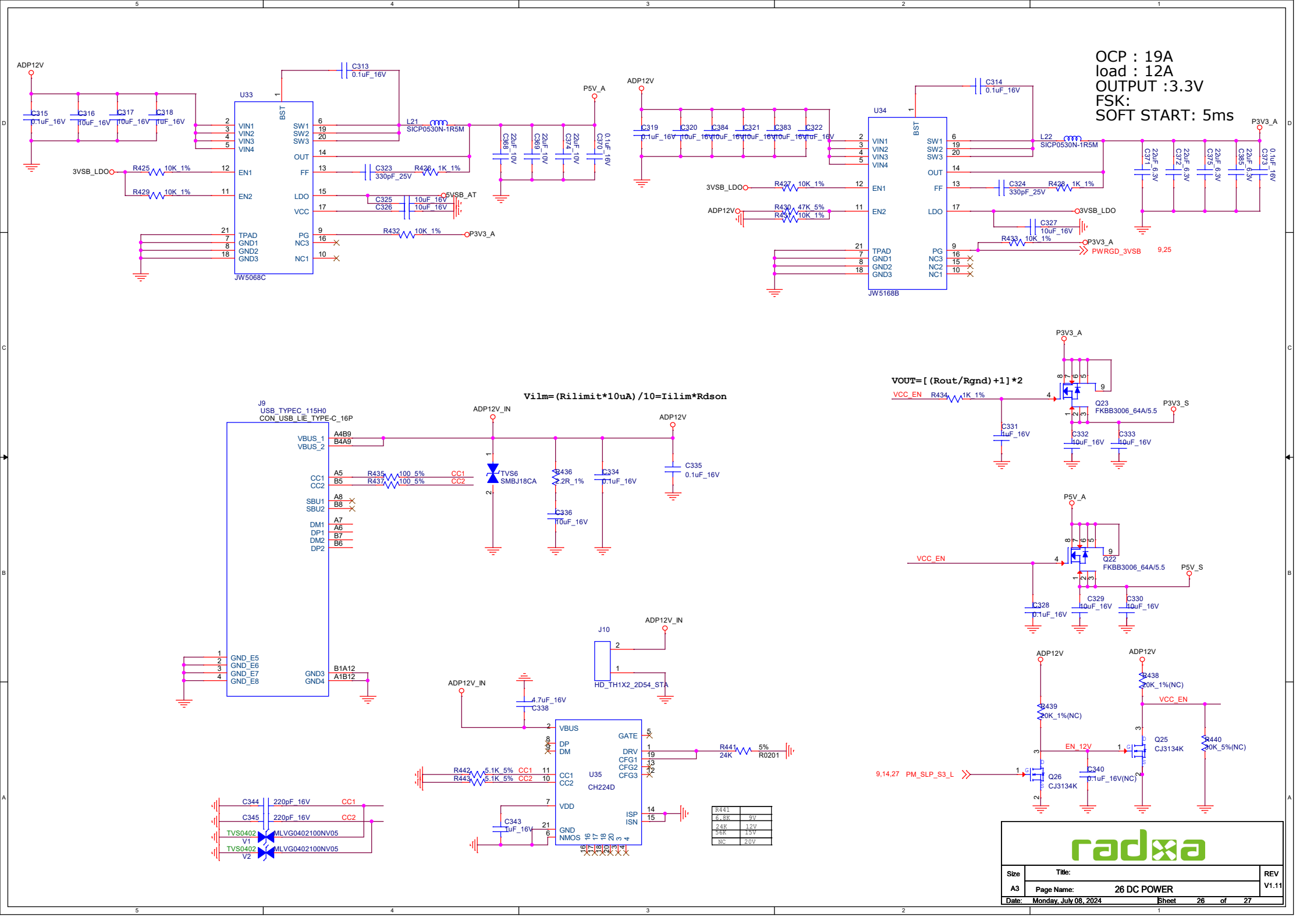
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	53.97K	330PF	53A
VCCGT	82.75K	220PF	29A
VCCIN_AUX	11K	220PF	27A

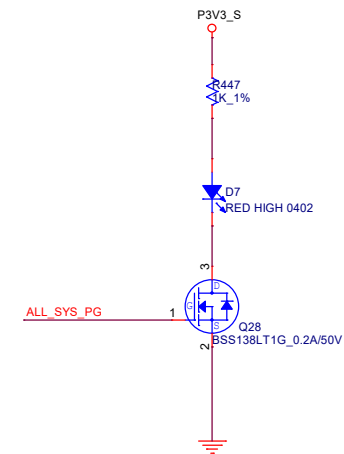
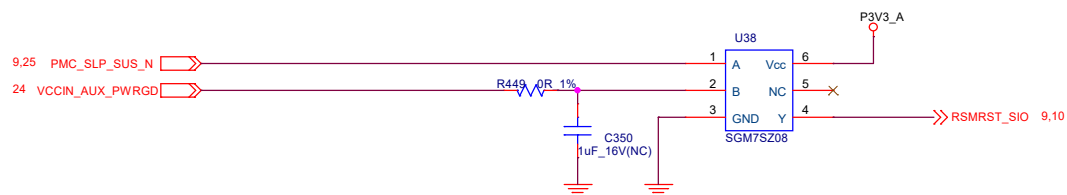
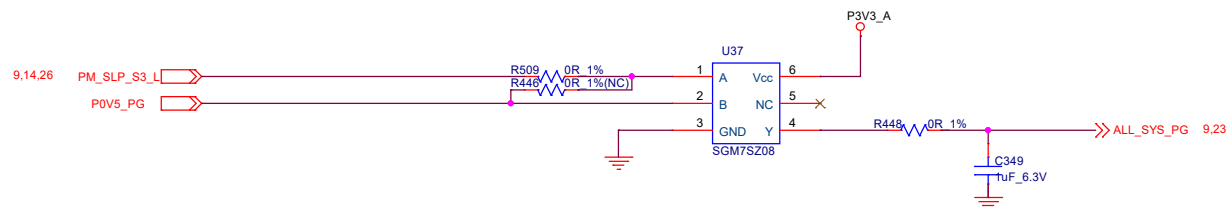
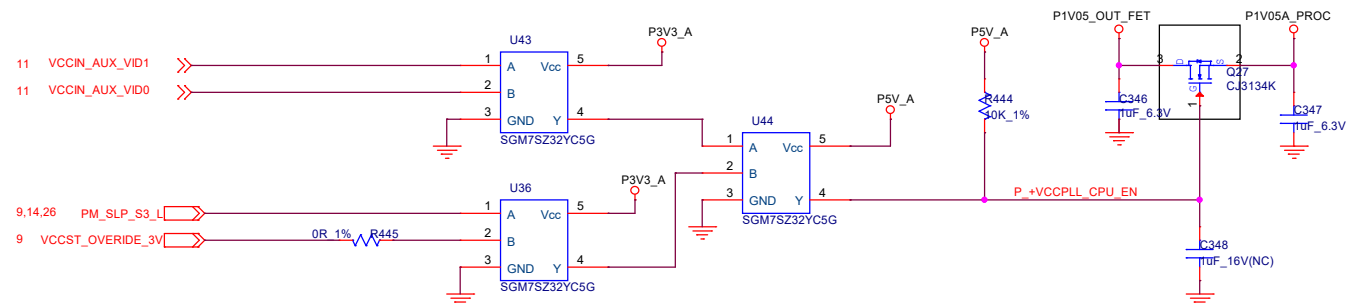


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